IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: NEMAZIE et al	Art Unit: 2181
Appl. No.: 10/775,523	Examiner: Lee, Chun
Filed: 02/09/2004	Atty. Docket: Siliconstor-0003CIP
For: Route Aware Serial Advanced Technology Attachment (SATA) Switch	

Amended Appeal Brief Under 37 CFR § 41.37

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Sir:

In response to the Office Communication mailed February 2/5/08, Appellants submit this amended appeal brief.

1- Please replace the Table of Contents, appearing on page two (2) of the Appeal Brief with the following Table of Contents:

Table of Contents

2- The independent claims are listed below, and mapped to specifications by page and line number and to the drawings.

Claim 1

Claim 1 A switch coupled between a plurality of host units and a device for routing frame information therebetween and comprising:

a. a first serial advanced technology attachment (ATA) port including a first host task file responsive to a non-data frame information structure (FIS) from a first host unit;

b. a second serial ATA port including a second host task file, responsive to a non-data FIS from a second host unit;

c. a third serial ATA port, responsive to a non-data FIS from a device; and

an arbitration and control circuit for selecting one of the first host or second host units to concurrently access the device, through the switch, by accepting non-data FIS, from either of the first or second host units, at any given time, including when the device is not in an idle state and whenever either one of the first or second host units sends non-data FIS to the device and further wherein the non-data FIS of the first and second host units and the device identify which one of the first or second host units is an origin and/or destination host so that routing of non-data FIS is transparent to the switch thereby reducing the complexity of the design of the switch rendering its manufacturing less expensive.

Subject Matter	Reference to Figs	Reference to Specs
A switch	Fig. 5 Block 200 FIg. 6 Block 300 Fig. 10a Block 500 Fig. 10b Block 500	Page 13, line 3 – Page 14, line 14 Page 15, lines 28 – 32 Page 35, lines 19 - 25
a plurality of host units	Fig. 3a items 11 and 12 Fig. 3b items 11 and 12	

a device	Fig. 3a item 16 Fig. 3b item 66	Page 1, lines 20 - 21
a first serial advanced technology attachment (ATA) port	Fig. 5 block 210 Fig. 6 blocks 310 Fig. 9 block 410. Fig. 10a block 510. Fig. 10b block 510	Page 13, line 16 – Page 14, line 14 Page 15 line 29 – Page 16 line 3 Page 27, lines 1 – 5 Page 34 line 18 – Page 35 line 19
a first host task file	Fig. 6, block labeled "Task File" inside block 310 Fig. 9, block 413a Fig. 10a, block 513a Fig. 10b, block labeled "FIS Holding Reg" inside block 510	Page 17, lines 19-20 Page 34, line 32 – Page 35, line 1 Page 45, lines 5-6 Page 45, lines 11- 13
a second serial ATA port	Fig. 5 block 220 Fig. 6 blocks 320 Fig. 9 block 410. Fig. 10a block 520. Fig. 10b block 520	Page 13, line 26 – Page 14, line 3 Page 15 line 30 – Page 16 line 7 Page 27, lines 6 – 10 Page 34 line 18 – Page 35 line 19
a second host task file	Fig. 6, block labeled "Task File" inside block 320 Fig. 9, block 413a Fig. 10a, block 523a Fig. 10b, block labeled "FIS Holding Reg"	Page 17, lines 19-20 Page 34, line 32 – Page 35, line 1 Page 45, lines 5-6 Page 45, lines 11- 13

	inside block 520	
a third serial ATA port, responsive to a non-data FIS from a device	Fig. 5 block 230 Fig. 6 blocks 330 Fig. 10a block 530. Fig. 10b block 530	Page 14, lines 4 – 14 Page 16, lines 7 – 11 Page 37, lines 17 - 18
an arbitration and control circuit for selecting one of the first host or second host units to concurrently access the device, through the switch, by accepting non-data FIS, from either of the first or second host units, at any given time, including when the device is not in an idle state and whenever either one of the first or second host units sends non-data FIS to the device and further wherein the non-data FIS of the first and second host units and the device identify which one of the first or second host units is an origin and/or destination host so that routing of non-data FIS is transparent to the switch thereby reducing the complexity of the design of the switch rendering its manufacturing less expensive		Page 15, lines 10 – 27 Page 16, line 12 – Page 19, line 6 Page 24, lines 1-5 Page 24, lines 7-12 Page 34, line 8 – Page 35, line 18 Page 35, line 31 – Page 37, line16 Page 37, line 18 – Page 39, line 10 Page 41, line 30 – Page 42, line 19 Page 44 lines 24 - 27

Claim 9

Claim 9: A switch comprising:

a. a first serial advanced technology attachment (ATA) port including a first host task file for connection to a first host unit, said first ATA port responsive to a non-data frame information structure (FIS) from the first host unit;

b. a second serial ATA port including a second host task file for connection to a second host unit responsive to a non-data FIS from the second host unit;

c. a third serial ATA port, responsive to a non-data FIS, for connection to a device, the switch for routing frame information between the first and second host units and the device; and

d. an arbitration and control circuit for selecting either the first host unit or the second host unit to concurrently access the device, through the switch, by accepting non-data FIS, from either of the first or second host units, at any given time, including when the device is not in an idle state, when either one of the first or second host units sends non-data FIS to the device,

wherein while one of the first or second host units is coupled to the device, through the switch, the other one of the first or second host units sends non-data FIS to the switch for routing to the device and further wherein the non-data FIS of the first and second host units and the device identify which one of the first or second host units is an origin and/or destination host so that routing of non-data FIS is transparent to the switch thereby reducing the complexity of the design of the switch rendering its manufacturing less expensive.

Subject Matter	Reference to Figs	Reference to Specs
A switch	Fig. 5 Block 200 FIg. 6 Block 300 Fig. 10a Block 500 Fig. 10b Block 500	Page 13, line 3 – Page 14, line 14 Page 15, lines 28 – 32 Page 35, lines 19 - 25
a fist host unit	Fig. 3a item 11 Fig. 3b item 11	
a second host unit	Fig. 3a item 12 Fig. 3b item 12	
a device	Fig. 3a item 16 Fig. 3b item 66	Page 1, lines 20 - 21
a first serial advanced technology attachment (ATA) port	Fig. 5 block 210	Page 13, line 16 – Page 14, line 14

	Fig. 6 blocks 310 Fig. 9 block 410. Fig. 10a block 510. Fig. 10b block 510	Page 15 line 29 – Page 16 line 3 Page 27, lines 1 – 5 Page 34 line 18 – Page 35 line 19
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a second serial ATA port	Fig. 5 block 220 Fig. 6 blocks 320 Fig. 9 block 410. Fig. 10a block 520. Fig. 10b block 520	Page 13, line 26 – Page 14, line 3 Page 15 line 30 – Page 16 line 7 Page 27, lines 6 – 10 Page 34 line 18 – Page 35 line 19
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a third serial ATA port, responsive to a non-data FIS, for connection to a device	Fig. 5 block 230 Fig. 6 blocks 330	Page 14, lines 4 – 14 Page 16, lines 7 – 11

	Fig. 10a block 530. Fig. 10b block 530	Page 37, lines 17 - 18
an arbitration and control circuit for selecting either the first host unit or the second host unit to concurrently access the device, through the switch, by accepting non-data FIS, from either of the first or second host units, at any given time, including when the device is not in an idle state, when either one of the first or second host units sends non-data FIS to the device, wherein while one of the first or second host units is coupled to the device, through the switch, the other one of the first or second host units sends non-data FIS to the switch for routing to the device and further wherein the non-data FIS of the first and second host units and the device identify which one of the first or second host units is an origin and/or destination host so that routing of non-data FIS is transparent to the switch thereby reducing the complexity of the design of the switch rendering its manufacturing less expensive.		Page 15, lines 10 – 27 Page 16, line 12 – Page 19, line 6 Page 24, lines 1-5 Page 24, lines 7-12 Page 34, line 8 – Page 35, line 18 Page 35, line 31 – Page 37, line16 Page 37, line 18 – Page 39, line 10 Page 41, line 30 – Page 42, line 19

Claim 14

Claim 14 (currently amended): A switch that is connectable to a first host unit, a second host unit and a device via serial advanced technology attachment (ATA) links, for routing frame information between the first and second host units and the device, said switch comprising:

a. a first serial ATA port, including a first host task file for connection to a first host unit, said first SATA port responsive to a non-data frame information structure (FIS) from the first host unit;

b. a second serial ATA port, including a second host task file for connection to a second host unit, responsive to a non-data FIS from the second host unit;

c. a third serial ATA port, responsive to a non-data FIS, for connection to a device;

d. an arbitration and control circuit for selecting one of the first or second host units to concurrently access the device through the switch, by accepting non-data FIS, from either of the first or second host units, at any given time, including when the device is not in an idle state, when either the first or second host units sends non-data FIS to the device,

wherein while one of the first or second host units is coupled to the device, the other one of to the first or second host units sends non-data FIS to the switch for routing to the device and further wherein the non-data FIS of the first and second host units and the device identify which one of the first or second host units is an origin and/or destination host so that routing of non-data FIS is transparent to the switch thereby reducing the complexity of the design of the switch rendering its manufacturing less expensive.

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A switch	Fig. 5 Block 200 FIg. 6 Block 300 Fig. 10a Block 500 Fig. 10b Block 500	Page 13, line 3 – Page 14, line 14 Page 15, lines 28 – 32 Page 35, lines 19 - 25
serial advanced technology attachment (ATA) links	Fig. 5, items 211rx 211tx, 231rx, 231tx, 221rd, 221tx Fig. 6, items 311rx, 311tx, 321rx, 321tx, 331rx, 331tx Fig. 9 items 411rx, 411tx Fig. 10a items 511tx, 511rx, 521tx, 521rx, 531tx, 531rx Fig. 10b items 511tx, 511rx, 521tx, 521rx, 531tx, 531rx	Page 13, lines 17 – 18, 26 - 29 Page 14, lines 5- 7 Page 15, line 32 – page 16 line 9 Page 36, lines 1-2, 9-10, 17 – 18 Page 37, lines 1 - 2, 9-10, 17 - 18
A first host unit	Fig. 3a item 11 Fig. 3b item 11	

A second host unit	Fig. 3a item 12 Fig. 3b item 12	
a device	Fig. 3a item 16 Fig. 3b item 66	Page 1, lines 20 - 21
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a first host task file	Fig. 6, block labeled "Task File" inside block 310 Fig. 9, block 413a Fig. 10a, block 513a Fig. 10b, block labeled "FIS Holding Reg" inside block 510	Page 17, lines 19-20 Page 34, line 32 – Page 35, line 1 Page 45, lines 5-6, 11- 13
a second serial ATA port	Fig. 5 block 220 Fig. 6 blocks 320 Fig. 9 block 410. Fig. 10a block 520. Fig. 10b block 520	Page 13, line 26 – Page 14, line 3 Page 15 line 30 – Page 16 line 7 Page 27, lines 6 – 10 Page 34 line 18 – Page 35 line 19
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a third serial ATA port, responsive to a non-data FIS, for connection to a device	Fig. 5 block 230 Fig. 6 blocks 330 Fig. 10a block 530. Fig. 10b block 530	Page 14, lines 4 – 14 Page 16, lines 7 – 11 Page 37, lines 17 - 18
an arbitration and control circuit for selecting one of the first or second host units to concurrently access the device through the switch, by accepting non-data FIS, from either of the first or second host units, at any given time, including when the device is not in an idle state, when either the first or second host units sends non-data FIS to the device, wherein while one of the first or second host units is coupled to the device, the other one of to the first or second host units sends non-data FIS to the switch for routing to the device and further wherein the non-data FIS of the first and second host units and the device identify which one of the first or second host units is an origin and/or destination host so that routing of non-data FIS is transparent to the switch thereby reducing the complexity of the design of the switch rendering its manufacturing less expensive		Page 15, lines 10 – 27 Page 16, line 12 – Page 19, line 6 Page 24, lines 1-5 Page 24, lines 7-12 Page 34, line 8 – Page 35, line 18 Page 35, line 31 – Page 37, line16 Page 37, line 18 – Page 39, line 10 Page 41, line 30 – Page 42, line 19

Claim 19

Claim 19 (currently amended): A method for communication between multiple host units and a device, through a serial advanced technology attachment (ATA) switch coupled to the multiple host units and the device using serial ATA links routing frame information therebetween comprising:

a. receiving a non-data frame information structure (FIS) through a first serial ATA port, from a first host unit;

b. receiving a non-data FIS, through a second serial ATA port, from a second host unit;

c. receiving a non-data FIS through a third serial ATA port;

d. arbitrating between the first and second host units and the device;

e. selecting one of the first or second host units for coupling to the device through the switch when either of the first or second host units sends commands for execution by the device;

f. coupling the device to the selected one of the first or second host units; and

g. while the selected one of the first or second host units is coupled to the device, the other one of the first or second host units sending non-data FIS to the switch for routing to the device

during the sending step g., the non-data FIS of the first and second host units and the device identifying which one of the first or second host units is an origin and/or destination host so that routing of non-data FIS is transparent to the switch thereby reducing the complexity of the design of the switch rendering its manufacturing less expensive.

Subject Matter	Reference to Figs	Reference to Specs
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serial advanced technology attachment (ATA) links	Fig. 5, items 211rx 211tx, 231rx, 231tx, 221rd, 221tx Fig. 6, items 311rx, 311tx, 321rx, 321tx, 331rx, 331tx Fig. 9 items 411rx,	Page 13, lines 17 – 18, 26 - 29 Page 14, lines 5- 7 Page 15, line 32 – page 16 line 9

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a third serial ATA port	Fig. 5 block 230 Fig. 6 blocks 330 Fig. 10a block 530. Fig. 10b block 530	Page 14, lines 4 – 14 Page 16, lines 7 – 11 Page 37, lines 17 - 18
the non-data FIS of the first and second host units and the device identifying which one of the first or second host units is an origin		Page 41, line 30 – Page 42, line 19

and/or destination host so that routing of non-data FIS is transparent to the switch		

Respectfully submitted,

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